REMARKS

Claims 1-40 are in this application.

Claim 1-40 have been canceled without prejudice or disclaimer.

Claims 1-28 have been canceled because they are drawn to a non-elected invention.

New claims 41-48 have been added.

Claims 41-48 are currently pending in this application.

Figures 1 and 2 have been amended as follows:

In Fig. 1, the solid black shading at **6** has been removed, the dark shading at **5** has been changed to a lighter shading and the straight arrows pointing to various elements have been changed to flexible arrows.

In Fig. 2, the solid black shading at **120**, **140**, **150** and **160** have been removed, the dark shading at **100** has been changed to a lighter shading, the straight arrows pointing to various elements have been changed to flexible arrows and the "poor line quality" has been improved by making the "lines, numbers and letters" of uniform thickness.

Replacement sheets are enclosed as an APPENDIX.

Amendments to the Drawings:

Figures 1 and 2 have been amended. Replacement sheets are enclosed as an APPENDIX. The Replacement sheets are identified in the top margin as "Replacement Sheet."

The Replacement sheets have been identified in the top margin of each sheet as being a "Replacement Sheet."

The specification has been amended by amending the "Abstract of the Disclosure" section to provide the missing information regarding the "interconnect structure."

Support for the new claims 41-48 is found in the canceled claims and in the following sections of the specification:

On page 9, line 18 to page 10, line 6, the specification states:

> "The dielectric may have k from 3.5 to 2, as described below. Below the dielectric **30** is a barrier/cap/etch stop layer **20** disposed atop a copper line below **100**. The dielectric layer **30** may include an optional hardmask layer **40** which may be composed of a single or multiple layers to form a composite hardmask film.
>
> All of the above components are disposed on a substrate **110**.
>
> After formation (by dry etching) of the openings **50** and **70**, attention is drawn to the bottom of the via opening, where the barrier/cap/etch stop layer **20** has an etched opening **90**. Opening **90** is known as the via bottom, where Cu **101** is exposed. The Cu surface may contain a Cu Oxide layer **120** due to Cu oxidation by the air, aqueous cleaning solution, partially oxygenated solvent cleaning solution, and other sources of oxygen such as the reactive feed gases used to form opening **90** in barrier/cap/etch stop layer **20**. The Cu Oxide layer **120** may contain carbon and other elements. Also present within the via opening may be a variable thickness of carbon residue **140**, which may contain H, F and other elements, may be polymeric or may be an amorphous carbon type material."

On page 6, line 19-25, the specification states:

> "In general, an integrated circuit will have interconnect levels, each level including metallic lines and vias that are of a dual damascene (via plus next level conductor) wiring interconnect structure for use on the IC chip. The metallic lines and vias are composed of the same or different conductive material. Suitable materials for use herein include, but are not limited to, W, Cu, Al, Ag, Au and alloys thereof and the like. A particularly preferred material is Cu."

On page 7, line 11-17, the specification states:

> "Generally, the hydrides and hydrogen sources are effective to remove oxide and oxygen containing residues, while fluorine sources are used to remove carbon containing residues. Preferably, the activation step can be carried out by bombarding with He+ ions, H2+ ions and/or H+/H2+ mixtures. Alternatively, the activation step can be carried out by irradiating with electron beam or irradiating with an ultraviolet (UV) radiation."

Claims 29-33 and 35-40 have been provisionally rejected under the judicially created doctrine of double patenting of the obviousness kind over the co-pending Applications Nos. 10/627,794 and 10/639,989.

Applicants acknowledge the provisional double patenting rejection and would consider filing an appropriate terminal disclaimer when allowable subject matter is indicated.

Claims 34 and 40 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Applicants have cancelled Claims 34 and 40. Therefore their rejection is moot.

Claims 29-33 and 35-40 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,884,123 to Dixit et al., herein after "Dixit" or U.S. Patent No. 6,358,832 to Edelstein et al., herein after " Edelstein."

Applicants have cancelled Claims 29-40. Therefore the rejection of 29-33 and 35-40 is moot.

The newly presented claims, namely claims 41-48, distinguish over Dixit and Edelstein as follows:

(1) In Dixit, the conductive layer that is contacted at the bottom of the "via" is the doped region in a Si or semiconductor substrate. In contrast to Dixit, the conductive layer that is contacted at the bottom of the "via" in the claimed interconnect structure is a metal, such as, W, Cu, Al, Ag, Au or alloys thereof. Thus, the structure of Dixit is different from the instantly claimed interconnect structure; and

(2) In Edelstein, there is no "via cleaning" step either taught or suggested. The use of a condensable cleaning agent or condensing a chemical in the via for the purpose of cleaning is not contemplated.

After the via opening is formed, the next step is to deposit a conductive liner (barrier) into the via openings. This results in an exposed conducting material having a surface that is contaminated by, for example, copper oxides, and other contaminants.

In contrast to Edelstein, the exposed surface of the conductive material in the etched openings in the instant invention has been treated with a condensable cleaning agent (CAA) and thereafter activated at a temperature about -200 °C to about 25 °C to remove oxide, oxygen and carbon containing residues from the exposed surface of the conductive material.

This is clearly described on page 9, line 26 to page 10, line 6, of the specification, which states:

> "After formation (by dry etching) of the openings **50** and **70**, attention is drawn to the bottom of the via opening, where the barrier/cap/etch stop layer **20** has an etched opening **90**. Opening **90** is known as the via bottom, where Cu **101** is exposed. The Cu surface may contain a Cu Oxide layer **120** due to Cu oxidation by the air, aqueous cleaning solution, partially oxygenated solvent cleaning solution, and other sources of oxygen such as the reactive feed gases used to form opening **90** in barrier/cap/etch stop layer **20**. The Cu Oxide layer **120** may contain carbon and other elements. Also present within the via opening may be a variable thickness of carbon residue **140**, which may contain H, F and other elements, may be polymeric or may be an amorphous carbon type material."

Therefore, in sharp contrast to Edelstein, the conductive layer that is contacted at the bottom of the "via" in the instantly claimed interconnect structure is free of such oxides and other impurities and residues because the exposed portion of the conductive material in the etched openings has been treated with a condensable cleaning agent (CCA) and activated at a temperature about -200 °C to about 25 °C prior to filling the vias with a conductive metal.

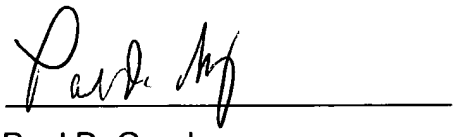
Accordingly, the exposed conducting material surface is free of contamination by materials, such as, for example, oxides, oxygen containing residues, carbon containing

residues and other residues and impurities because the exposed surface of the conductive material has been treated with a condensable cleaning agent (CCA) and activated at a temperature about -200 °C to about 25 °C prior to filling the vias with a conductive metal.

Based on the foregoing, currently pending claims, namely claims 41-48, are patentable over the cited art for at least the reasons set forth herein above.

Accordingly, reconsideration, withdrawal of the objections and rejections and allowance of claims 41-48 are respectfully requested.

Respectfully submitted,

Date: January 5, 2005 By: 

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